System Configuration Guide

Chapter 4

4.1 Introduction

This chapter describes the modules required to assemble typical systems using model 4100 series components and gives the necessary interconnections. In addition to the main units you will also need a ready supply of suitable 50 Ω BNC cables, BNC "tee" pieces and BNC 50 Ω terminators. Such items, if not already to hand, are widely available from electronics component suppliers.

4.2 System Configurations

4.2.01 Single Channel Static Gate Manual System

Required Equipment:

- Model 4121B Boxcar Averager
- NIM Bin and power supply, such as model 4001A/4002D

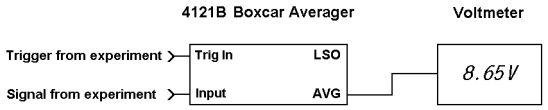

Figure 4-1, Single Channel Static Gate Manual System

The system is shown above in figure 4-1.

The 4121B is mounted in the NIM bin (not shown) and the trigger and signal from the experiment applied to it. The internal trigger delay generator is used to set the gate position at the required point on the signal waveform and the output averager controls are adjusted to give the required output stability. A voltmeter is used to monitor the measured signal.

4.2.02 Single Channel Waveform Recording System using ADC/DAC PC Card

Required Equipment:

- Model 4121B Boxcar Averager
- NIM Bin and power supply, such as model 4001A/4002D
- PC interface card offering at least one ADC input and one DAC output with ±10 V FS range, 12 bits or better (not available from ***SIGNAL RECOVERY***)

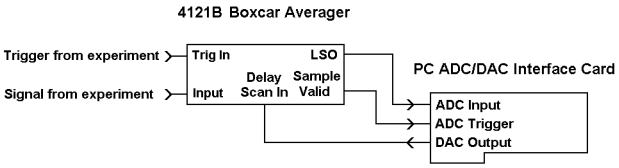

Figure 4-2, Single Channel Waveform Recording System using ADC/DAC PC Card

The system is shown above in figure 4-2.

In this case the DAC output of a third-party ADC/DAC plug-in card for a PC is used to generate a control voltage for the internal trigger delay generator of the 4121B, which is housed in the NIM bin (not shown). The 4121B's last sample output is cabled to the card's ADC input, and the sample valid output is used as an external trigger input for the card's ADC. User-developed software generates a staircase ramp waveform at the DAC output that sweeps the sampling gate across the desired delay range, and at each step acquires and digitally averages the required number of sample values. The resulting waveform record is stored to file for subsequent display and analysis.

4.2.03 Single Channel System with Baseline Subtraction

Required Equipment:

- Model 4121B Boxcar Averager
- NIM Bin and power supply, such as model 4001A/4002D
- Optical Chopper with external reference frequency input to set chopping frequency, such as the ***SIGNAL RECOVERY*** model 197 or 650 series.

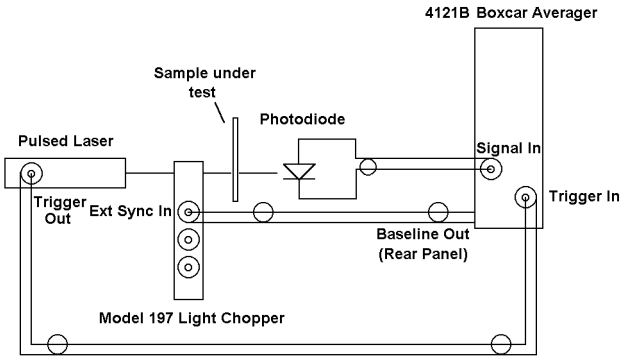

Figure 4-3, Single Channel System with Baseline Subtraction

The system is shown above in figure 4-3.

A pulsed laser running at 1 kHz is passed through a model 197 light chopper to the sample under test and thence to the photodiode detector. The 4121B, which is housed in the NIM bin (not shown), is set to the Baseline 1 sampling mode and triggered from the laser. In this mode, the **BASELINE I/O (TTL)** line on the 4121B is an output

which with a 1 kHz trigger rate will be at 500 Hz. This output is connected to the model 197 light chopper's external sync input, causing the chopper to run at 500 Hz. With suitable positioning this means that alternate laser pulses do not reach the sample, so that alternate samples correspond to "signal" and "baseline" values.

The 4121B performs an automatic subtraction of these samples to give automatic baseline removal.

4.2.04 Two Channel Static Gate System with GPIB Interface

Required Equipment:

- Two Model 4121B Boxcar Averagers
- One Model 4161A Dual ADC and Display Module
- NIM Bin and power supply, such as model 4001A/4002D

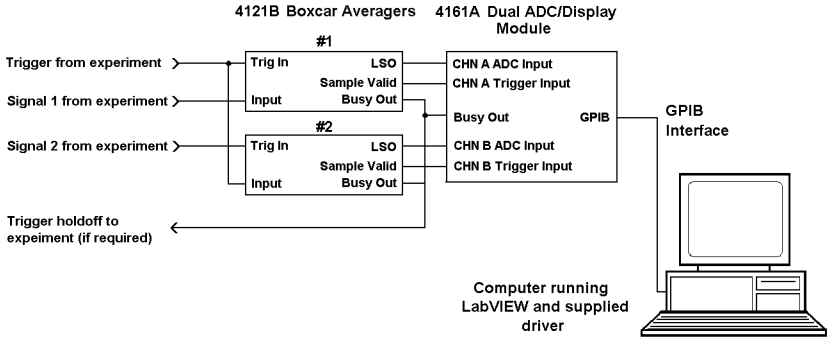

Figure 4-4, Two Channel Static Gate System with GPIB Interface

The system is shown above in figure 4-4.

One model 4161A ADC module is used to digitize the outputs generated by two model 4121B boxcar averagers, with all three units being mounted in the NIN bin (not shown). The computer controls the rate of acquisition via the 4161A. In cases of high trigger rates (typically greater than 50 - 100 Hz) the 4161A's **BUSY OUT (TTL)** output can be used to holdoff the experimental trigger to allow the computer to control the number of trigger cycles.

4.2.05 Four Channel Waveform Recording System using Model 9650A DDG

Required Equipment:

- Four Model 4121B Boxcar Averagers
- Two Model 4161A Dual ADC and Display Modules
- ***SIGNAL RECOVERY*** Model 9650A four channel digital delay generator fitted with /97 GPIB interface option
- NIM Bin and power supply, such as model 4001A/4002D

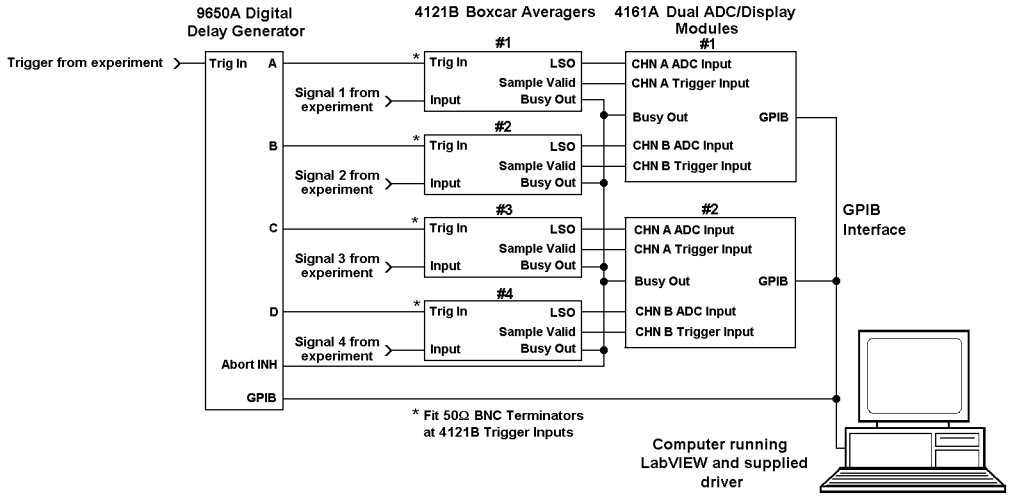

Figure 4-5, Four Channel Waveform Recording System using Model 9650A DDG

The system is shown above in figure 4-5.

Two model 4161A ADC modules are used to digitize the outputs generated by four model 4121B boxcar averagers, with all six units being mounted in the NIN bin (not shown). In addition a model 9650A four channel digital delay generator fitted with a GPIB interface is used to generate delayed triggers to each of the four boxcar averagers.

The 9650A output levels should be set to +5 V and connected to the trigger inputs of the 4121B's. In order to avoid errors due to trigger pulse reflection it is advisable to use 50 Ω terminators at the 4121B end of each trigger cable.

The computer controls the rate of acquisition via the 4161A, by means of the **BUSY OUT (TTL)** output. This is used to holdoff the trigger to the system by preventing the 9650A from triggering whenever data is still being processed from an earlier trigger.

Specifications

Appendix A

Model 4121B Boxcar Averager

General

Single-channel gated integrator module mounted in NIM enclosure with adjustable sensitivity, offset, gatewidth and output averager. Manual controls.

Analog gate delay generator with manual or DC voltage control.

Measurement Modes

On receipt of an external trigger, the instrument waits for the preset gate delay and then integrates the voltage present at its input for the preset gate width. On completion a DC voltage representing this integral is provided at the Last Sample Output connector and in addition fed forward into an analog integrator stage.

Signal Channel

Mode	Normal or Baseline Sampling
Sensitivity	±20 mV to ±2 V in 1-2-5 sequence
Coupling	AC/DC
Impedance	
DC only	50 Ω // 10 pF
DC or AC	1 MΩ // 30 pF
Maximum Safe Input	
50 Ω Input	±5 V
1 MΩ Input	±100 V
Offset	
20 mV - 200 mV sensitivity	±10 × FS; non-removable
500 mV - 2 V sensitivity	±2 V; non-removable
Overload Indicator	LED
Overload Level	Input (signal plus noise) > 1.1 × FS
Overload Recovery	Recovers after 1 sample for ×10 overload
Gain Drift	0.5 % /°C, gate width > 30 ns; 1.0 % /°C, gate width < 10 ns
DC Drift (referred to input)	
	0.2 %/°C, gate width > 20 ns; 1.0 %/°C, gate width < 20 ns
Bandwidth	
50 Ω input	DC to 450 MHz
1 MΩ DC input	DC to 100 MHz
1 MΩ AC input	1.5 Hz to 100 MHz
Signal Risetime	
50 Ω input	2 ns; 20 % to 80 %
1 MΩ input	10 ns; 20 % to 80 % from 50 Ω source.

Sampler and Timing

Gate Width	1 ns to 30 µs in 1-3-10 sequence, switch selectable with a continuously variable ×1 to ×5 multiplier
Sample Correlation	Less than 0.5% of the sample output due to trigger *t* remains at trigger *t* + 1
Gate Delay	
Input	0 to 10 V DC varies delay by 0.5 % to 100 % of range setting
Max delay	3 ns to 300 ns in 1-3-10 sequence plus user options, which give 10 µs (default), and 1 µs, 100 µs, 1 ms or 3 ms by capacitor change.
Trigger Source	
Internal	0.5 Hz to 40 kHz selectable with range switches 0.5, 5, 50, 500 5000, off. Vernier is 10× range.
External	
ECL	Positive edge, 5 ns min pulse width with termination of 50 Ω to -2 V; -5 V to +10 V pk-pk safe input.
TTL	Positive edge, 20 ns min pulse width; -5 V to +10 V safe input.
Max. Trigger Rate	80 kHz
Trigger Indicator	LED lights when unit is triggered
Trigger Generator	
Output	BNC TTL out on rear panel active in all trigger modes. Polarity set by jumper.
Frequency ranges	0.5, 5, 50, 500 Hz, 5 kHz and OFF with vernier to overlap ranges.
Baseline Input	TTL line to indicate whether sample is signal or baseline value.

Analog Output Averager

Mode	Linear or Exponential
Averager Reset	Front-panel push button or ground applied to **RESET AVG I/O** rear-panel input
Samples Averaged	1, 3, 10, 30, 100, 300, 1k, 10k
LSO Droop Rate	< 0.2 % FS/s
Averager Droop Rate	When there are no triggers the droop rate is < 0.001 % per minute for 10k samples

Outputs

Average Out	±10 V FS with 50 Ω output impedance and capable of driving 2 kΩ load
Last Sample Out	±10 V FS
Gate Monitor	0.3 V into 50 Ω to ground. Marker pulse-width equals gate width. Position is within 5 ns of actual gate

Internal Oscillator	TTL
Baseline Output	TTL output line that toggles with each trigger to indicate whether next sample is signal or baseline value.

General

Power Requirements	
	+24 V at 200 mA; -24 V at 150 mA +12 V at 300 mA; -12 V at 590 mA +6 V at 160 mA; -6 V at 630 mA
Dimensions	
Height	8¾" (222 mm)
Width	2¾" (70 mm)
Depth	9¾" (248 mm)
Weight	3 lb (1.4 kg)

Model 4161A Dual Channel ADC & Display Module

General

Two-channel ADC mounted in NIM enclosure with signal and trigger inputs and with trigger holdoff output. RS232 and GPIB (IEEE488) control. Separate analog edge-indicating panel meter.

Input

Channels	Two
ADC Inputs	BNC front-panel connectors, A and B
Input Impedance	1 MΩ
Input Full-Scale	±10 V
Accuracy	±5 mV
Linearity	±5 mV
ADC Trigger Inputs	BNC front-panel connectors, corresponding to channel A and channel B ADC inputs. Connectors are duplicated on rear panel
Trigger Thresholds	TTL. Triggers on rising edge of applied positive logic TTL pulse

Digital Display

Type	3½ digit LED display showing (Measured voltage / 20)
Display Selection	Switch selects channel A or channel B

Computer Interfaces

RS232	DIP switch selectable baud rate, terminator, character echo, parity and data bits.
GPIB	DIP switch selectable address and terminator
Status Indicators	Front panel LEDs indicate GPIB Talk, Listen, SRQ and Remote
Command Set	Seventeen mnemonic type commands allowing both asynchronous and synchronous readings. Digitized voltages are reported back to the computer in integer format, with ±2048 corresponding to an input voltage of ±10.24 V
Software	LabVIEW driver software suitable for version 4.01 and later of LabVIEW is available by download from our website at **www.signalrecovery.com**

Output

Busy Out	Rear-panel BNC connector generating TTL signal which under computer control will:- 1) Remain at logic 0 until a synchronized read command is issued by the computer. 2) Go to logic 1, releasing external trigger hold-off circuitry (such as can be provided by the ***SIGNAL RECOVERY*** model 9650A) 3) Return to logic 0 on receipt of a trigger signal at either the A or B ADC trigger inputs, and remain there while the measured value(s) are transferred back to the computer and thereafter until the next synchronized read command.

Analog Panel Meter

Type	Edge-indicating meter monitoring the voltage at the associated front-panel analog input BNC connector. This meter is completely independent of the analog to digital converter functions.
Input Impedance	10 kΩ
Full-scale sensitivity	±10 V

General

Power Requirements	
	+24 V at 50 mA; -24 V at 50 mA +12 V at 600 mA; -12 V at 30 mA +6 V at 550 mA; -6 V at 10 mA
Dimensions	
Height	8¾" (222 mm)
Width	2¾" (70 mm)
Depth	9¾" (248 mm)
Weight	2½lb (1.14 kg)