PhaseLock

Universal and compact phase stabilization electronics

- Compact, stand-alone locking electronics for pulsed lasers
- Pulse timing stabilization
- 2 independent PID regulators
- High-voltage output for piezo actuators
- Lock point validity detection and automatic "search" function
- Multi-channel monitor for display of regulator signals
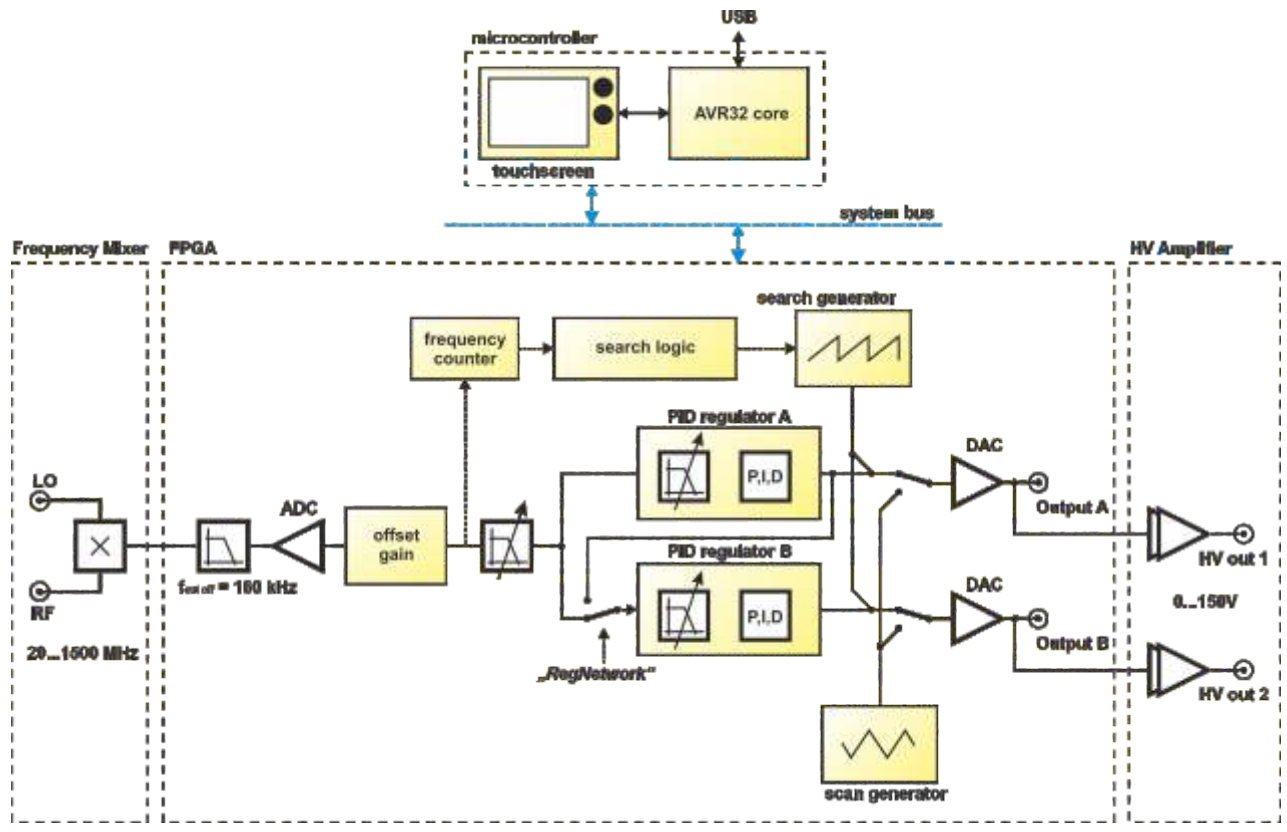
Application

- Stabilization of the repetition rate and pulse timing of pulsed lasers
- Phase locking of the optical frequency of continuous lasers
- Control of the pulse envelope phase (carrier offset frequency) of femtosecond lasers
- Stabilization of frequency or phase of electronic oscillators

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Block Diagram

PhaseLock combines all components required for or beneficial to phase stabilization in a user-friendly compact device:

- fast input amplifiers
- phase comparator
- 2 independent PID regulators, adapted especially to resonant systems like piezo-driven optical components
- scan generator, for adjustment or supervision of the physical system
- output amplifier, user-selectable as high-voltage amplifier for piezo actuators, or as low-voltage amplifier generating a control signal for external amplifier sections
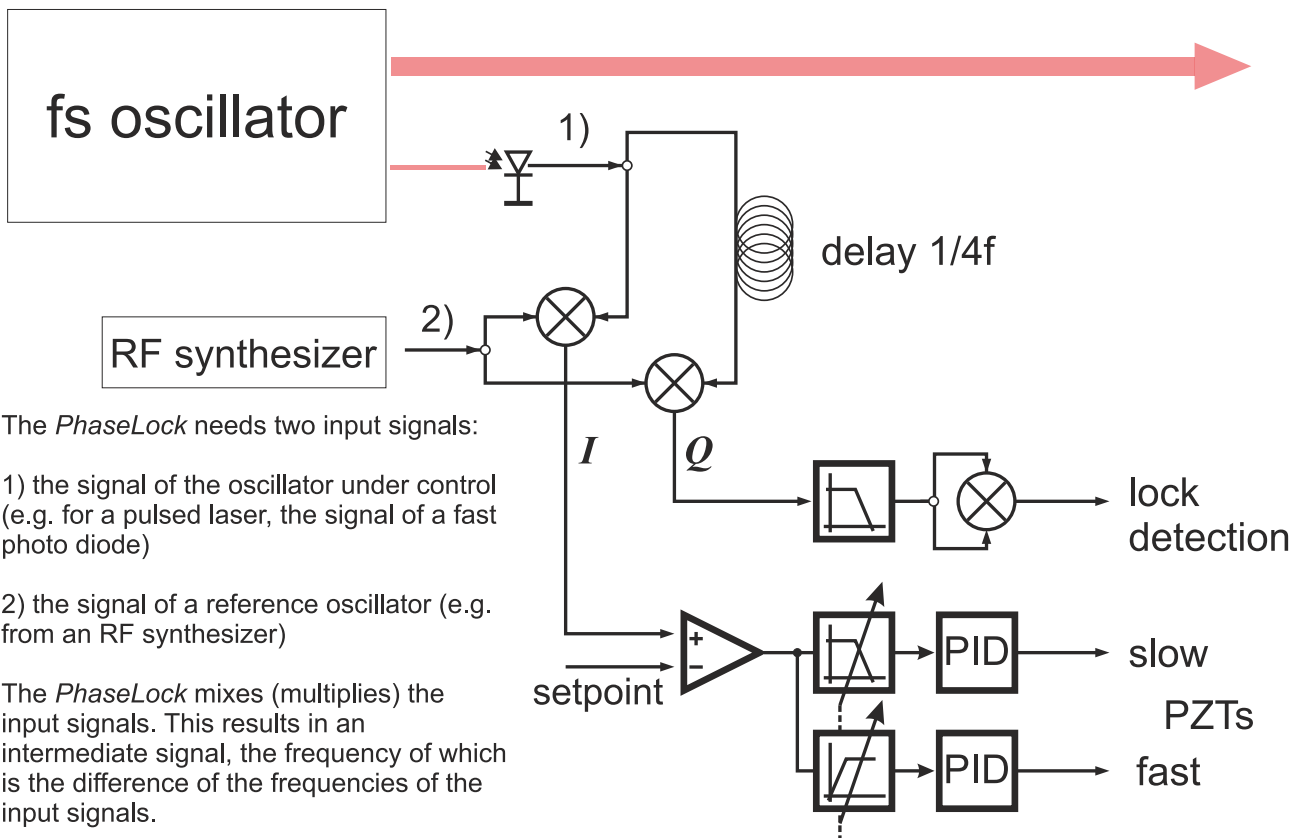- logic section for automatic recognition of successful locking

Signal Diagram

If the frequency difference of the input signals is too large, a simple PID controller will not be able to align the input frequencies within one cycle of the difference signal. Then, the control loop will fail to lock. In order to avoid this problem, the PhaseLock is equipped with a discriminator: As long as the frequency difference is higher than a preset value, the output voltage ramps through its full range. As soon as the frequency difference is lower than a preset value ("frequency lock window"), the PID loop is closed.

lock window
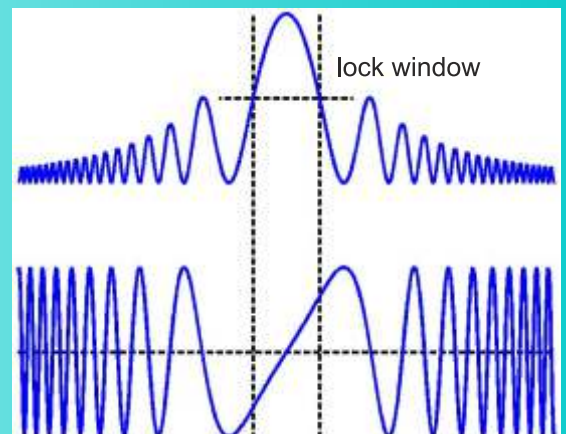
Application Example

The *PhaseLock* compares the phase of an RF input signal with a local oscillator (LO).

fs oscillator

1)

delay 1/4f

RF synthesizer

2)

The *PhaseLock* needs two input signals:

1) the signal of the oscillator under control (e.g. for a pulsed laser, the signal of a fast photo diode)

2) the signal of a reference oscillator (e.g. from an RF synthesizer)

The *PhaseLock* mixes (multiplies) the input signals. This results in an intermediate signal, the frequency of which is the difference of the frequencies of the input signals.
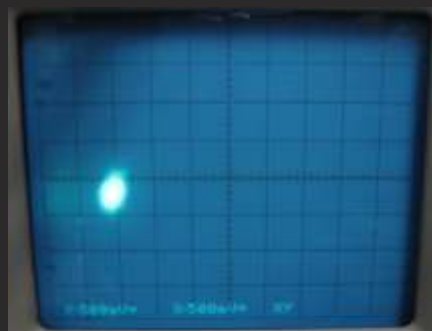
I Q

lock detection

setpoint

PID — slow PZTs

PID — fast

a) IQ (quadrature) mixer output (while unlocked)

b) Phase memory analog output (while unlocked). The amplitude of 10Vpp corresponds to full 8192 cycles!

c) IQ (quadrature) mixer output when locked

Option MCPC

If phase excursions exceed $+/-\pi$, a conventional RF mixer loses cycles. This results in phase slips, which is sometimes not acceptable. In order to avoid this problem, the *PhaseLock* can be equipped with a phase counter, which acts as a "memory" for lost cycles (option MCPC). The output of this add-on circuit is an analog voltage proportional to the phase difference within a range as large as $+/-8192\pi$. This provides a long time for the PID servo loop to settle, thus enabling phase locks even in diffcult situations in which standard locking schemes would fail.

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Technical Data

Signal inputs	Impedance:	50 Ohm
	RF bandwidth	1GHz
	Input power	LO: +13dBm
	IF Bandwidth	300kHz (standard, higher BW on request)
	Sampling Rate	2.5MS/s
Option MCPC	Phase memory (cycles)	$+/-4096 \cdot 2\pi$
Outputs	Voltage range	+/- 10V at 1kOhm load
	Impedance	50 Ohm
	Sampling Rate	2.5MS/s
Drivers (optional)	HV amplifier	2x 150V, 50mA, BNC
Lock detection	Frequency window	adjustable
Twin PID regulator	combinations	independent / parallel / series
	over-all delay	400ns
Scan generator	Output frequency	100mHz ... 20kHz (triangular shape)
Supply	Voltage range	100..120V / 220..240V AC, 50..60Hz
Housing	Dimensions HxWxD	88mmx260mmx373mm
Display	Size	4.3"
	Resolution	480x272
	Colors	65 536 (16 bit)

Costumer specific values on request. Subject to change without notice.

Development, Manufacturing and Distribution

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