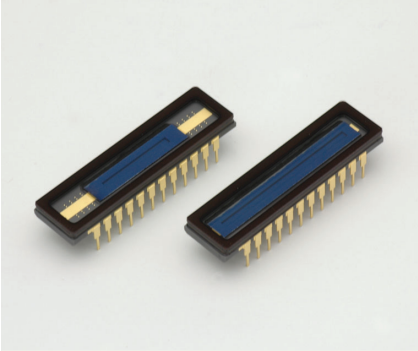
HAMAMATSU
PHOTON IS OUR BUSINESS

IR-enhanced CCD image sensors



S11510 series

Enhanced near infrared sensitivity: QE=40% (λ=1000 nm)

The S11510 series is a family of FFT-CCD image sensors for photometric applications that offer improved sensitivity in the near infrared region at wavelengths longer than 800 nm. Our unique technology in laser processing was used to form a MEMS structure on the back side of the CCD. This allows the S11510 series to have much higher sensitivity than our previous products (S10420-01 series).
In addition to having high infrared sensitivity, the S11510 series can be used as an image sensor with a long active area in the direction of the sensor height by binning operation, making it suitable for detectors in Raman spectroscopy. Binning operation also ensures even higher S/N and signal processing speed compared to methods that use an external circuit to add signals digitally.
The S11510 series has a pixel size of 14 × 14 µm and is available in two image areas of 14.336 (H) × 0.896 (V) mm (1024 × 64 pixels) and 28.672 (H) × 0.896 (V) mm (2048 × 64 pixels). The S11510 series is pin compatible with the S10420-01 series, and so operates under the same drive conditions.

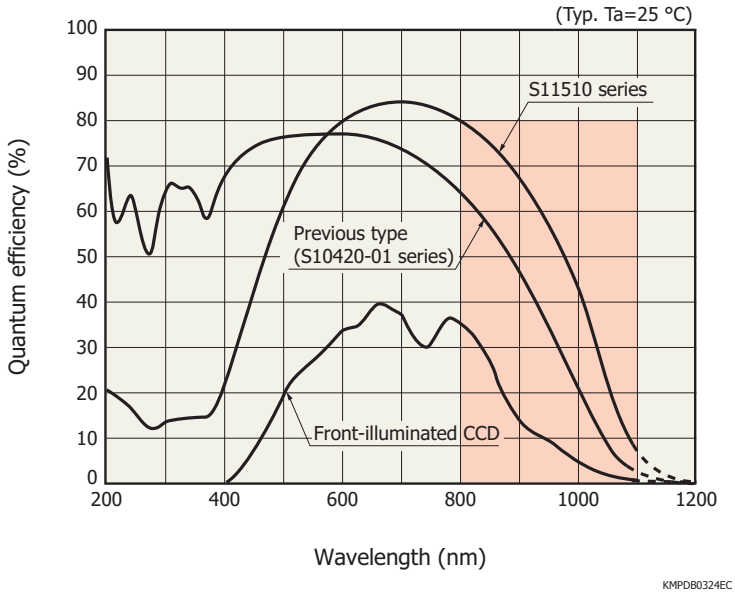
Features

- **Enhanced near infrared sensitivity: QE=40% (λ=1000 nm)**
- **High CCD node sensitivity: 6.5 µV/e⁻**
- **High full well capacity and wide dynamic range (with anti-blooming function)**
- **Pixel size: 14 × 14 µm**
- **MPP operation**

Applications

- **Raman spectrometers, etc.**

Spectral response (without window)*1



*1: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

Structure

Parameter	S11510-1006	S11510-1106
Pixel size (H × V)	14 × 14 µm	
Number of total pixels (H × V)	1044 × 70	2068 × 70
Number of effective pixels (H × V)	1024 × 64	2048 × 64
Image size (H × V)	14.336 × 0.896 mm	28.672 × 0.896 mm
Vertical clock phase	2-phase	
Horizontal clock phase	4-phase	
Output circuit	One-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outline)	
Window	Quartz glass*2	
Coooling	Non-cooled	

*2: Resin sealing

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*3	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
Output transistor drain voltage	V_{OD}	-0.5	-	+30	V
Reset drain voltage	V_{RD}	-0.5	-	+18	V
Over flow drain voltage	V_{OFD}	-0.5	-	+18	V
Vertical input source voltage	V_{ISV}	-0.5	-	+18	V
Horizontal input source voltage	V_{ISH}	-0.5	-	+18	V
Over flow gate voltage	V_{OFG}	-10	-	+15	V
Vertical input gate voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
Horizontal input gate voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
Summing gate voltage	V_{SG}	-10	-	+15	V
Output gate voltage	V_{OG}	-10	-	+15	V
Reset gate voltage	V_{RG}	-10	-	+15	V
Transfer gate voltage	V_{TG}	-10	-	+15	V
Vertical shift register clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal shift register clock voltage	V_{P1H}, V_{P2H} V_{P3H}, V_{P4H}	-10	-	+15	V

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

*3: Package temperature

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	23	24	25	V
Reset drain voltage			V_{RD}	11	12	13	V
Over flow drain voltage			V_{OFD}	11	12	13	V
Over flow gate voltage			V_{OFG}	0	12	13	V
Output gate voltage			V_{OG}	4	5	6	V
Substrate voltage			V_{SS}	-	0	-	V
Test point	Input source		V_{ISV}, V_{ISH}	-	V_{RD}	-	V
	Vertical input gate		V_{IG1V}, V_{IG2V}	-9	-8	-	V
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	V
Vertical shift register clock voltage		High	V_{P1VH},V_{P2VH}	4	6	8	V
		Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH} V_{P3HH}, V_{P4HH}	4	6	8	V
		Low	V_{P1HL}, V_{P2HL} V_{P3HL}, V_{P4HL}	-6	-5	-4	
Summing gate voltage		High	V_{SGH}	4	6	8	V
		Low	V_{SGL}	-6	-5	-4	
Reset gate voltage		High	V_{RGH}	4	6	8	V
		Low	V_{RGL}	-6	-5	-4	
Transfer gate voltage		High	V_{TGH}	4	6	8	V
		Low	V_{TGL}	-9	-8	-7	
External load resistance			R_L	90	100	110	kΩ

Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	0.25	0.5	MHz
Vertical shift register capacitance	-1006	C_{P1V}, C_{P2V}	-	600	-	pF
	-1106		-	1200	-	
Horizontal shift register capacitance	-1006	C_{P1H}, C_{P2H} C_{P3H}, C_{P4H}	-	80	-	pF
	-1106		-	160	-	
Summing gate capacitance		C_{SG}	-	10	-	pF
Reset gate capacitance		C_{RG}	-	10	-	pF
Transfer gate capacitance	-1006	C_{TG}	-	30	-	pF
	-1106		-	60	-	
Charge transfer efficiency*4		CTE	0.99995	0.99999	-	-
DC output level		Vout	17	18	19	V
Output impedance		Zo	-	10	-	kΩ
Power consumption*5		P	-	4	-	mW

*4: Charge transfer efficiency per pixel, measured at half of the full well capacity
*5: Power consumption of the on-chip amplifier plus load resistance

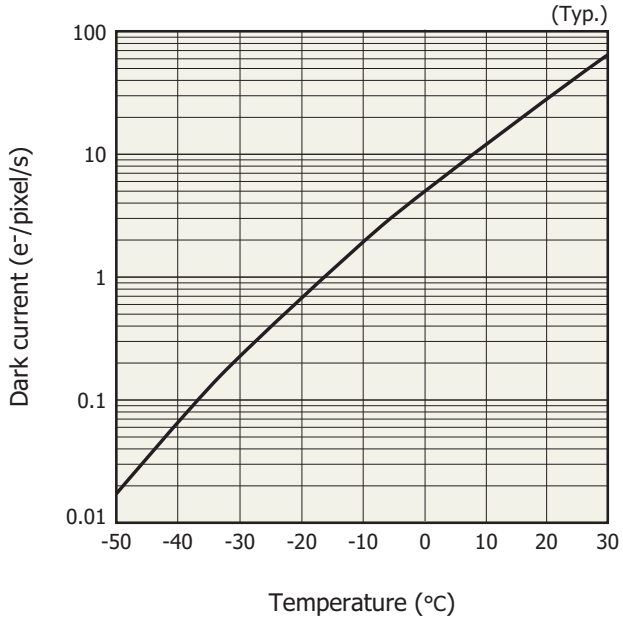
Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	50	60	-	ke^-
	Horizontal		250	300	-	
CCD node sensitivity		Sv	5.5	6.5	7.5	$\mu V/e^-$
Dark current*6		DS	-	50	200	e^-/pixel/s
Readout noise*7		Nr	-	6	15	e^- rms
Dynamic range*8	Line binning	DR	41700	50000	-	-
Spectral response range		λ	-	200 to 1100	-	nm
Photoresponse nonuniformity*9		PRNU	-	±3	±10	%

*6: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*7: Temperature: -40 °C, readout frequency: 20 kHz
*8: Dynamic range = Full well capacity / Readout noise
*9: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \ [\%$$

Dark current vs. temperature



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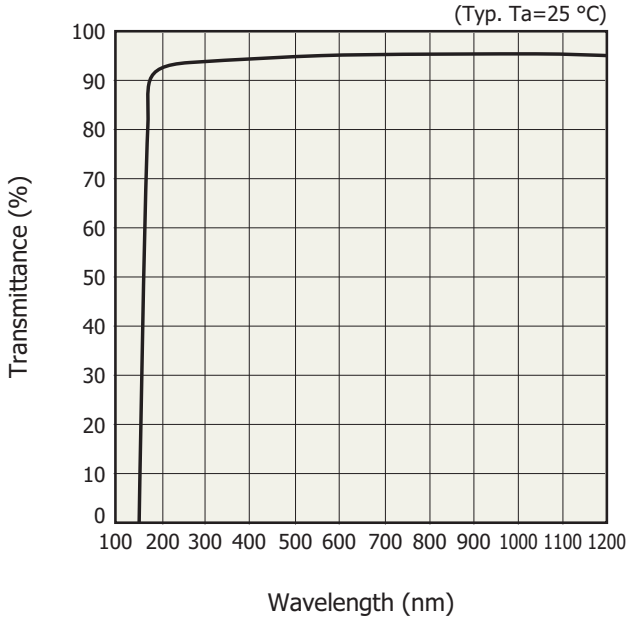
Spectral transmittance characteristic of window material



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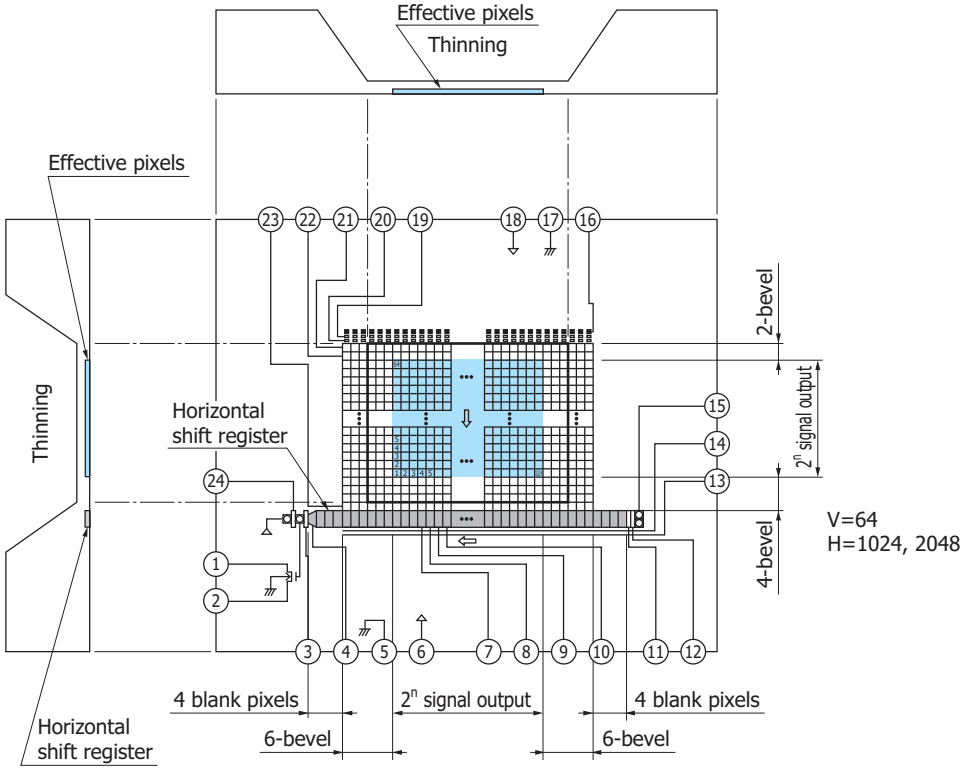
Device structure (conceptual drawing of top view in dimensional outline)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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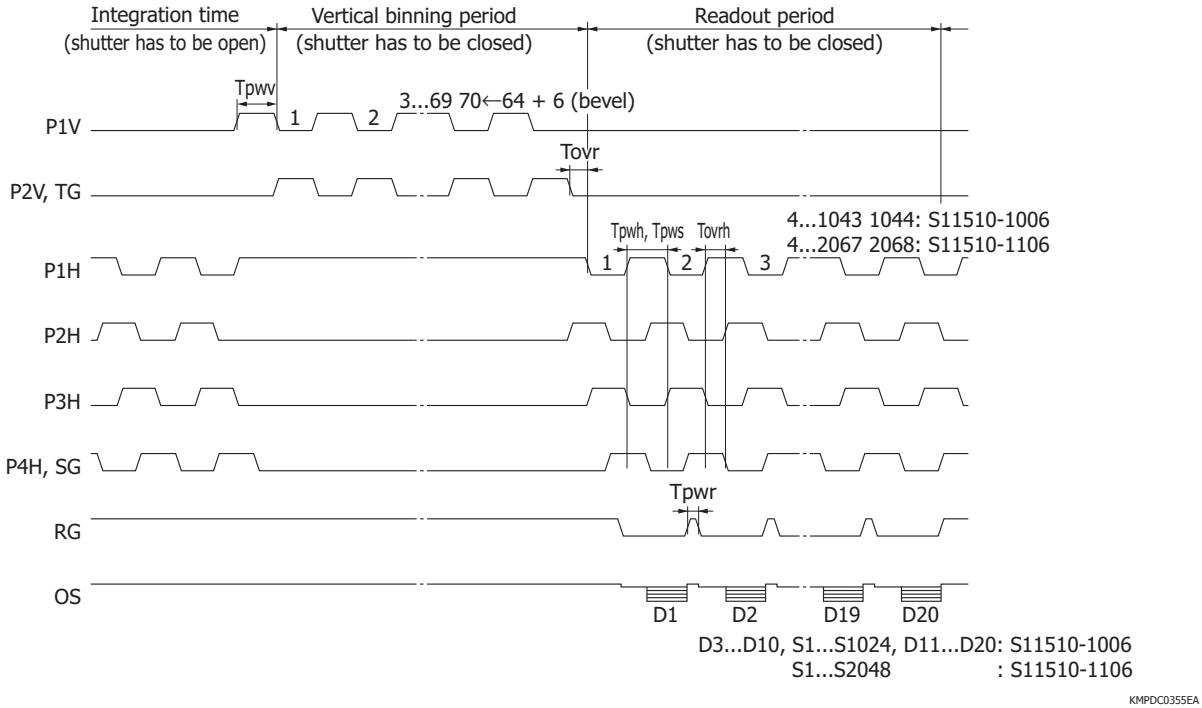
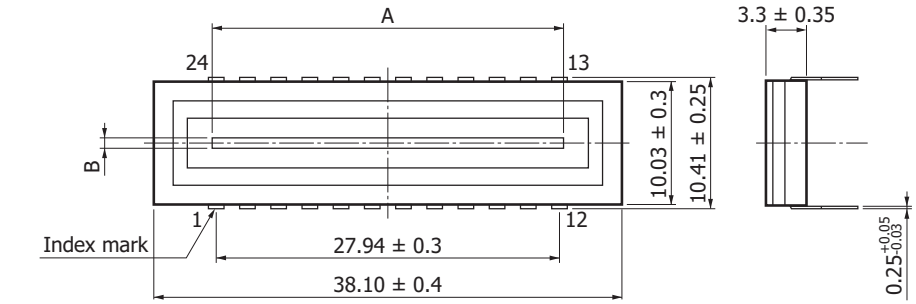
Timing chart (line binning)

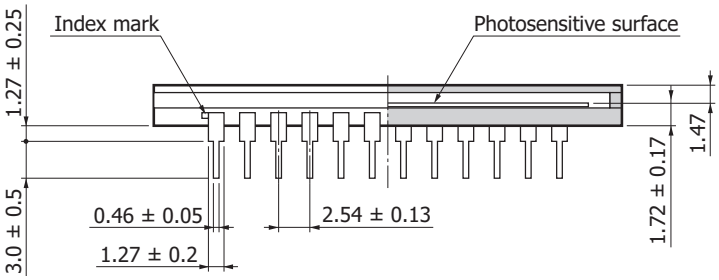


Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width*10	Tpwv	6	8	-	µs
	Rise and fall times*10	Tprv, Tpfv	20	-	-	ns
P1H, P2H, P3H, P4H	Pulse width*10	Tpwh	1000	2000	-	ns
	Rise and fall times*10	Tprh, Tpfh	10	-	-	ns
	Pulse overlap time	Tovrh	500	1000	-	ns
	Duty ratio*10	-	40	50	60	%
SG	Pulse width*10	Tpws	1000	2000	-	ns
	Rise and fall times*10	Tprs, Tpfs	10	-	-	ns
	Pulse overlap time	Tovrh	500	1000	-	ns
	Duty ratio*10	-	40	50	60	%
RG	Pulse width	Tpwr	100	1000	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG-P1H	Overlap time	Tovr	1	2	-	µs

*10: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)





Type no.	Photosensitive area	
	A	B
S11510-1006	14.336 (H)	0.896 (V)
S11510-1106	28.672 (H)	0.896 (V)

KMPDA0265EA

Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	R_L=100 kΩ
2	OD	Output transistor drain	+24 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	SS	Substrate	GND
6	RD	Reset drain	+12 V
7	P4H	CCD horizontal register clock-4	
8	P3H	CCD horizontal register clock-3	
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	-8 V
12	IG1H	Test point (horizontal input gate-1)	-8 V
13	OFG	Over flow gate	+12 V
14	OFD	Over flow drain	+12 V
15	ISH	Test point (horizontal input source)	Connect to RD
16	ISV	Test point (vertical input source)	Connect to RD
17	SS	Substrate	GND
18	RD	Reset drain	+12 V
19	IG2V	Test point (vertical input gate-2)	-8 V
20	IG1V	Test point (vertical input gate-1)	-8 V
21	P2V	CCD vertical register clock-2	
22	P1V	CCD vertical register clock-1	
23	TG	Transfer gate	Same pulse as P2V
24	RG	Reset gate	

Precautions (electrostatic countermeasures)

- When handling CCD sensors, always wear a wrist strap and also anti-static clothing, gloves, and shoes, etc. The wrist strap should have a protective resistor (about 1 MΩ) on the side closer to the body and be grounded properly. Using a wrist strap having no protective resistor is hazardous because you may receive an electrical shock if electric leakage occurs.
- Avoid directly placing these sensors on a work bench that may carry an electrostatic charge.
- Provide ground lines with the work bench and work floor to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

- Notice
- Image sensors/Precautions

■ Technical information

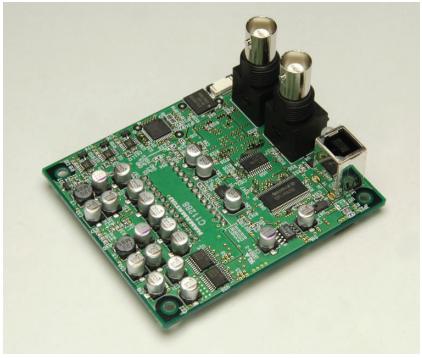
- FFT-CCD area image sensor/Technical information

Driver circuit for CCD image sensor (S11510 series) C11287 [sold separately]

The C11287 is a driver circuit designed for HAMAMATSU CCD image sensors S11510 series. The C11287 can be used in spectrometers, etc. when combined with the CCD image sensor.

Features

- **Built-in 14-bit A/D converter**
- **Interface to computer: USB 2.0**
- **Power supply: USB bus power operation**



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